What is claimed is:

1. A method for parallel testing of memory on a plurality of wireless devices, comprising:

issuing a command to each wireless device to test its memory;

retrieving the results of the command to test memory; and

identifying one or more wireless devices with failed memory.

2. The method of claim 1, further comprising communicating with the wireless devices using a Bluetooth™ protocol, or any embedded wireless RF protocol.

3. The method of claim 1, further comprising communicating with the wireless devices using one or more pads on the devices as antennas.

4. The method of claim 1, further comprising communicating with the wireless devices using one or more traces on the devices as antennas.

5. The method of claim 1, further comprising communicating with the wireless devices using one or more power traces on the devices as antennas.

6. The method of claim 1, further comprising performing wafer sort tests on the wireless devices.

7. The method of claim 1, further comprising performing parametrics tests on the wireless devices.

8. The method of claim 1, further comprising collecting memory test results from the wireless devices and displaying test results on a computer.

9. The method of claim 1, further comprising erasing test software from the memory of each wireless device.

10. The method of claim 9, further comprising reclaiming memory for the test software for operating software on each wireless device.

11. A system, comprising:

one or more wireless devices, each device including:

a processor; and

memory coupled to the processor; and

a tester adapted to exercise the wireless devices, including:

a transceiver adapted to communicate with each wireless device; and

a computer coupled to the transceiver, the computer adapted to test all wireless devices in parallel by issuing a single test command using a wireless signal, the computer adapted to store test patterns and test results.

12. The system of claim 11, wherein each processor is coupled to a multi-mode wireless circuit on a single substrate.

13. The system of claim 12, wherein each multi-mode wireless circuit comprises:

an analog portion integrated on the substrate, including:

a cellular radio core;

a radio sniffer coupled to the cellular core; and

a short-range wireless transceiver core coupled to the cellular core, the short-range wireless transceiver core being adapted to receive signals from the tester without an external antenna; and

a digital portion integrated on the substrate, including:

a reconfigurable processor core coupled to the cellular radio core and the short-range wireless transceiver core, the reconfigurable processor adapted to handle a plurality of wireless communication protocols; and

a high-density memory array core coupled to the reconfigurable multi-processor core, including a start-up code memory and a non-volatile FLASH memory.

14. The system of claim 12, wherein the protocol conforms to a Bluetooth™ or any embedded wireless RF protocol.

15. The system of claim 11, wherein the short-range wireless transceiver core is adapted to receive signals from an on-chip antenna.

16. The system of claim 11, wherein the short-range wireless transceiver core is adapted to receive signals from an on-chip pad, wire or power trace.

17. The system of claim 11, wherein the memory array core is adapted to receive built-in-self-test code.

18. The system of claim 11, wherein the memory array core is adapted to receive parametrics test code.

19. The system of claim 11, wherein the wireless devices are formed on a wafer, further comprising:

a power line deposited on the wafer during processing and adapted to be removed after wafer dicing; and

a plurality of switches coupled to the devices and the power line to allow each wireless device on the wafer to be tested in a sequence.

20. The system of claim 11, wherein a portion of the memory array core storing the test code is freed to store data after testing operation.